MMDA Qualification Issues

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Need for MMDA

- **Accelerating pace of new and more complex waveforms**

- **Cost of Qualification of New waveforms**

- **Cost of Re-qualification for existing hardware and software for upgrades and modifications**

- **Increased cost of new system development**

- **Re-configurability of avionics systems for various geo locations**

- **Over Ocean Communications**

- **Air Traffic Control Free Flight in 2015-2020**

- **Compatibility and interoperability with existing waveforms**
  - *IEE Standards*
  - *EuroCAE and ARINC Standards*
  - *Military Standards*
  - *SEI Software Standards*
  - *CORBA Frame Architecture*

Need for a new design requires updated approaches for design and qualification

Functional Approach: What is an MMDA

- ## Multi-Mode
  - *Multiple Modes of a Single Radio Type in a Single LRU*

- ## Multi-Function
  - *More than one Communication Function in LRU*
  - *Communication, Navigation and/or Surveillance Functions in a single LRU*

- ## Prototype Functionality
  - *Demonstrate both Multi-Mode and Multi-Functionality*

**Utilize Common Hardware and Software Architecture
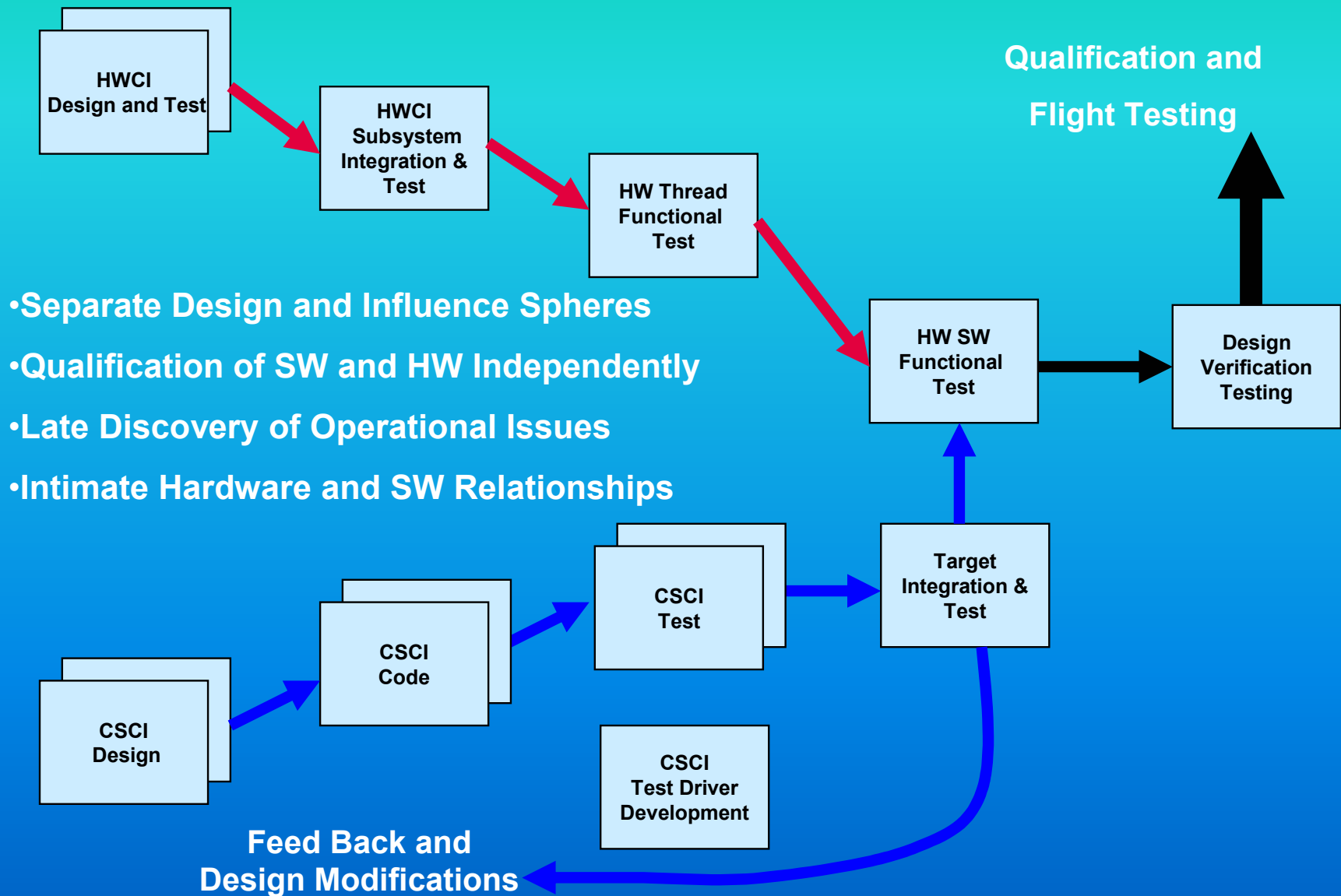for future enhancements**

Key Elements of MMDA Approach

Blend Military and Commercial products into multi-mode, multi-function cost effective commercial radio design

- Utilize DoD investment in JTRS and SAE Software technology as Leverage to Commercial Air Traffic Control applications

  – *Boeing 777*   *- JTRS*

  – *Air Bus 3XX*   *- F-22 Integrated Avionics*

  – *RAH-66 Integrated Avionics*   *-JSF Integrated Avionics*

- Data Link Capability has key functionality but must meet the bandwidth and throughput requirements for Air Traffic Densities in 2015

  – *VDR Mode 3 with growth to mode 4*

  – *UAT*

  – *Implement IP over Link-16*

  – *Bandwidth-on-Demand Advantages*

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Traditional Waterfall Development

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HWCI Design and Test → **HWCI Subsystem Integration & Test** → **HW Thread Functional Test** → **HW SW Functional Test** → **Design Verification Testing** → **Qualification and Flight Testing**

- Separate Design and Influence Spheres
- Qualification of SW and HW Independently
- Late Discovery of Operational Issues
- Intimate Hardware and SW Relationships

CSCI Design → **CSCI Code** → **CSCI Test** → **Target Integration & Test**

CSCI Test Driver Development

Feed Back and Design Modifications
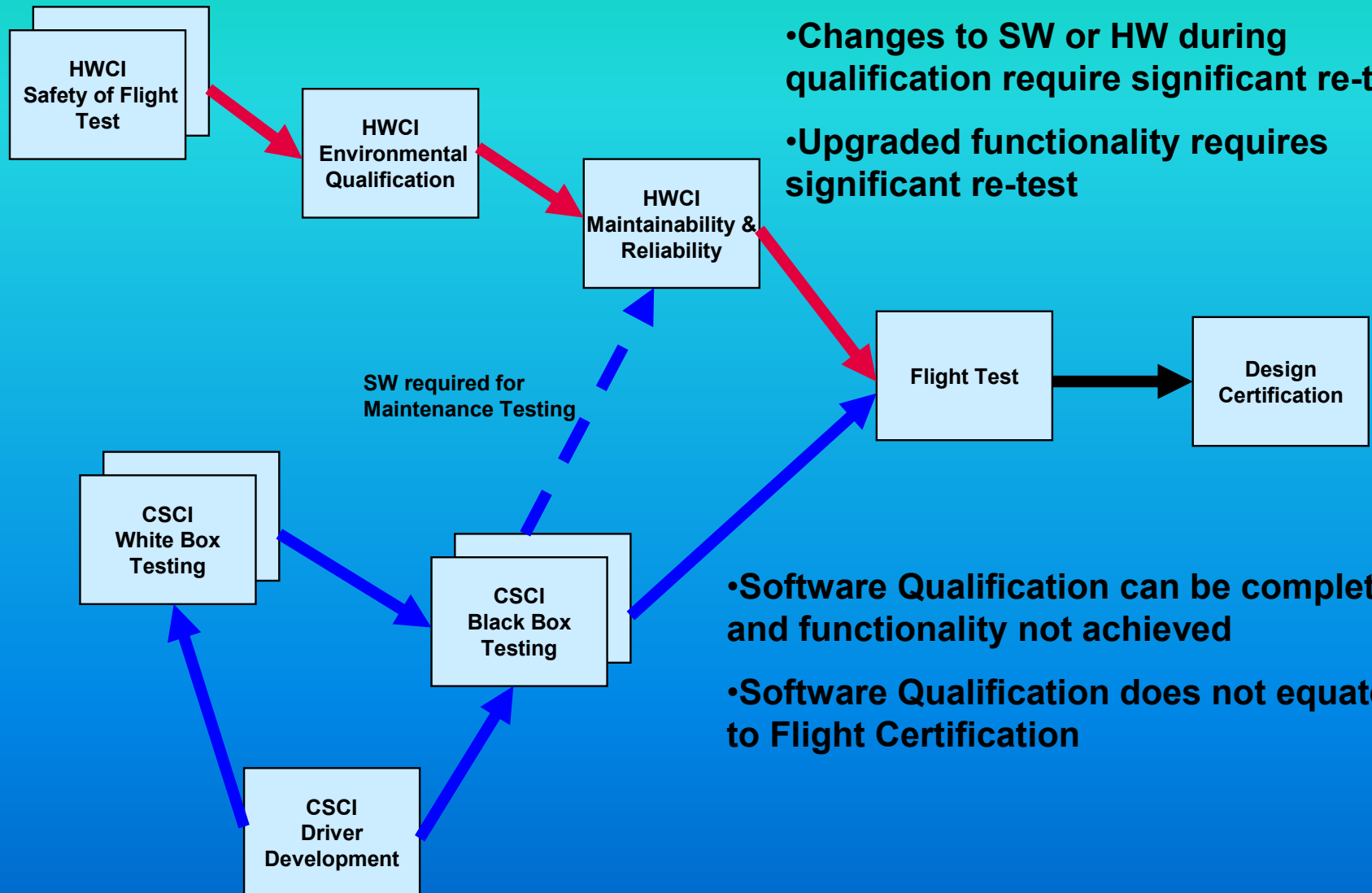
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Waterfall Design Approach Critical Problems

- **Assumption that coding is wasted if started prior to the completion and approval of design**

- **Serialization of tasks cause significant changes and re-design**

  - *Late discovery of requirements cause significant re-coding and regression testing*
  - *Cost and Schedule Risk increases*

Traditional Waterfall Qualification

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```
HWCI
Safety of Flight
Test
```
→
```
HWCI
Environmental
Qualification
```
→
```
HWCI
Maintainability &
Reliability
```
→
```
Flight Test
```
→
```
Design
Certification
```

SW required for Maintenance Testing

```
CSCI
White Box
Testing
```
→
```
CSCI
Black Box
Testing
```

```
CSCI
Driver
Development
```

- **Changes to SW or HW during qualification require significant re-test**

- **Upgraded functionality requires significant re-test**

- **Software Qualification can be completed and functionality not achieved**

- **Software Qualification does not equate to Flight Certification**

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Waterfall Qualification Critical Problems

- **Hardware and Software qualification often pursue separate tracks**

  - *Hardware qualification centers on Environmental, EMI and Safety of flight*
  - *Software is tested separately to provide clear independence from hardware*
  - *Functional testing reveals performance issues late in the qualification schedule*

- **Upgrades and changes to software create significant cost and schedule risk due to extensive regression testing**
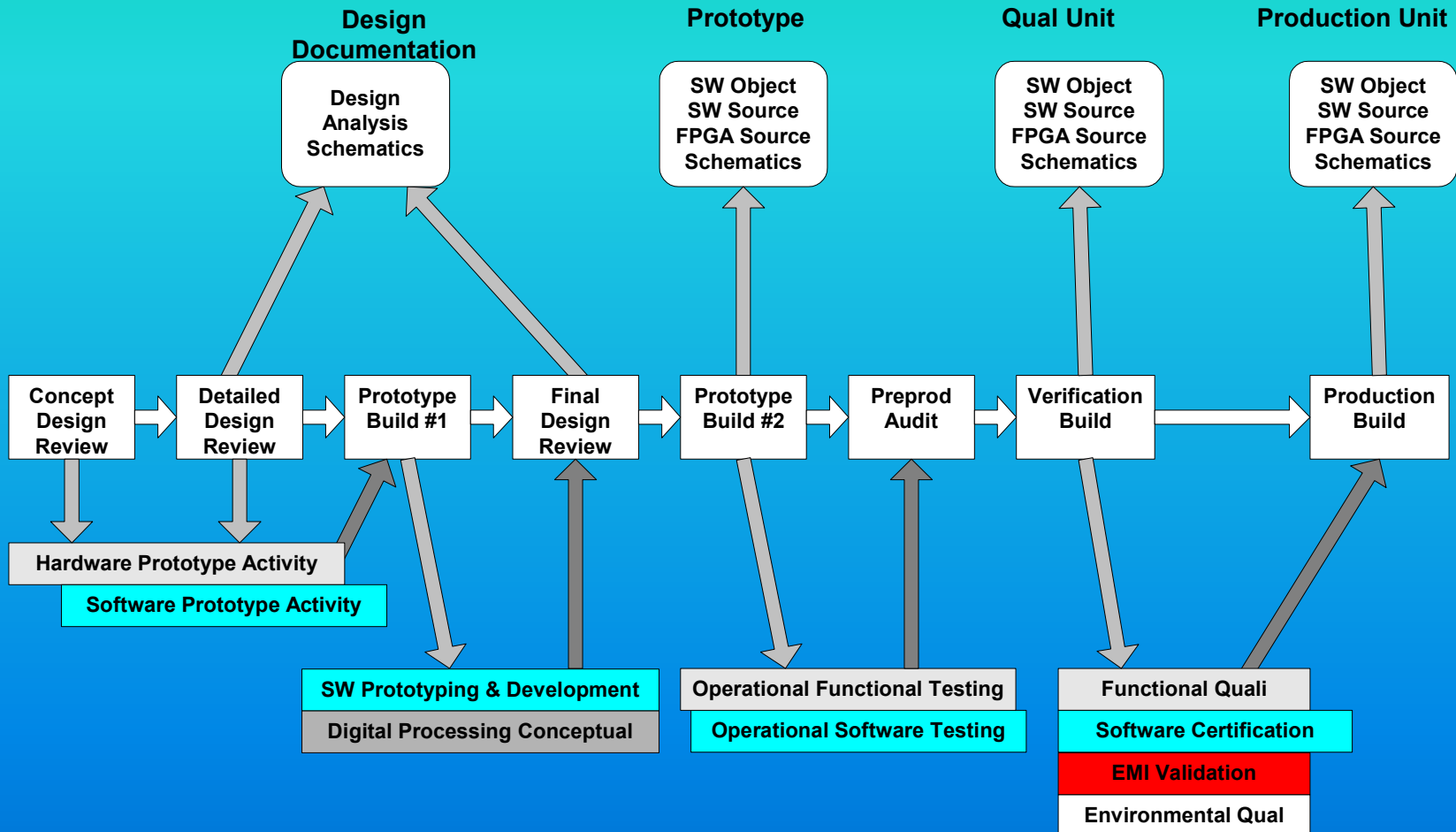
Proposed Iterative Processes

- **Multiple build and test cycles to allow both hardware and software to mature prior to final product deployment**

- **Each iteration includes test objectives and demonstration**
  - *Test results are used to incorporate design adjustments at the next phase*

- **Identification early in design process of key technical performance measures**
  - *Test and measurements at each iteration to track progress*

- **Newly discovered requirements incorporated at next design iteration**

- **Reduces qualification risk through early hardware and software integration**

- **Incorporates design changes prior to critical qualification process**

Incremental Build & Qualification

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Design Documentation

Prototype

Qual Unit

Production Unit

Design Analysis Schematics	SW Object SW Source FPGA Source Schematics	SW Object SW Source FPGA Source Schematics	SW Object SW Source FPGA Source Schematics

Concept Design Review	Detailed Design Review	Prototype Build #1	Final Design Review	Prototype Build #2	Preprod Audit	Verification Build	Production Build

Hardware Prototype Activity

Software Prototype Activity

SW Prototyping & Development

Digital Processing Conceptual

Operational Functional Testing

Operational Software Testing

Functional Quali

Software Certification
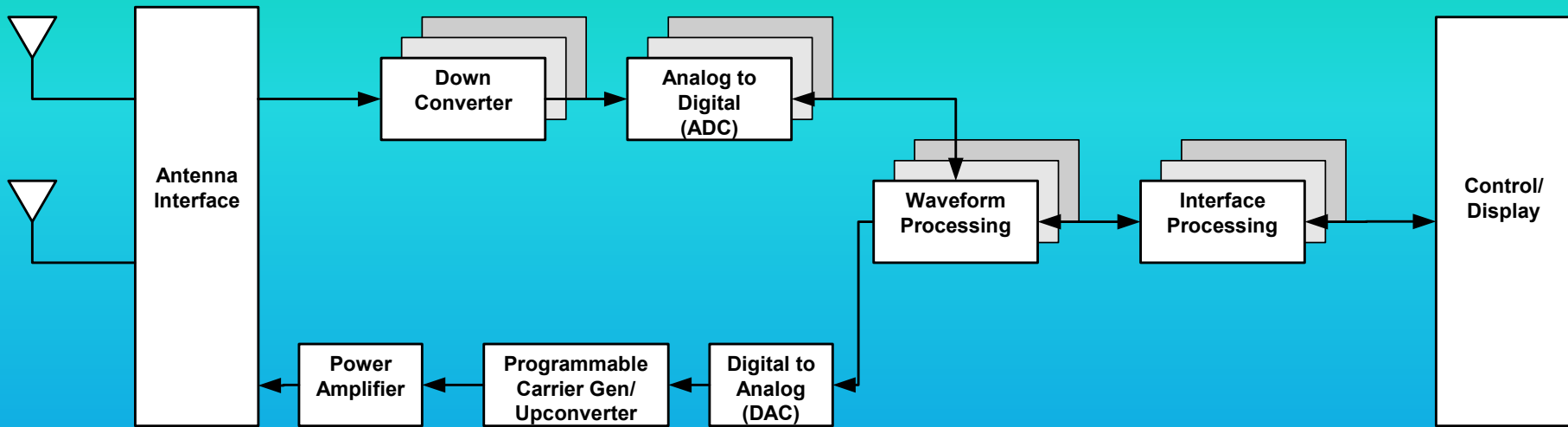
EMI Validation

Environmental Qual

Incremental Design and Risk Reduction

- **Each phase of Hardware Development have a corresponding integration phase**
  - *Specific Risk reduction items are required prior to continuing development tasks.*

- **High risk reduction tasks are accomplished early in the development cycle**
  - *Design modifications identified prior to expensive flight testing*
  - *Collect HWCI and CSCI data for future functional verification*

- **Early prototype hardware is utilized as software prototyping test bed**
  - *Software development continues on target hardware*
  - *Software performance enhancements throughout the course of development*

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MMDA Candidate Architecture

```
Antenna
Interface → Down Converter → Analog to Digital (ADC) → Waveform Processing → Interface Processing → Control/Display

Control/Display → Interface Processing → Waveform Processing → Digital to Analog (DAC) → Programmable Carrier Gen/Upconverter → Power Amplifier → Antenna Interface
```

One or more Power Amps or a Multi-mode Power Amp dependent on Functionality within MMDA

- **Common Hardware/Open Architecture**
- **Commercial Level Cryptography**
- **SEI/SCA Based Software Architecture**
- **OSIL/CORBA implementation**

Multiple functionality and performance in the presence of failures

MMDA Performance Challenges

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- ## RF
  - *Multiple Power Levels*
  - *Multiple Antenna Configurations*
  - *Spectral purity*
  - *Pulse shaping*
  - *Linearity*
  - *EMC Features*
  - *Dynamic Range*
  - *Interference Rejection*
  - *Hard-limited IF*

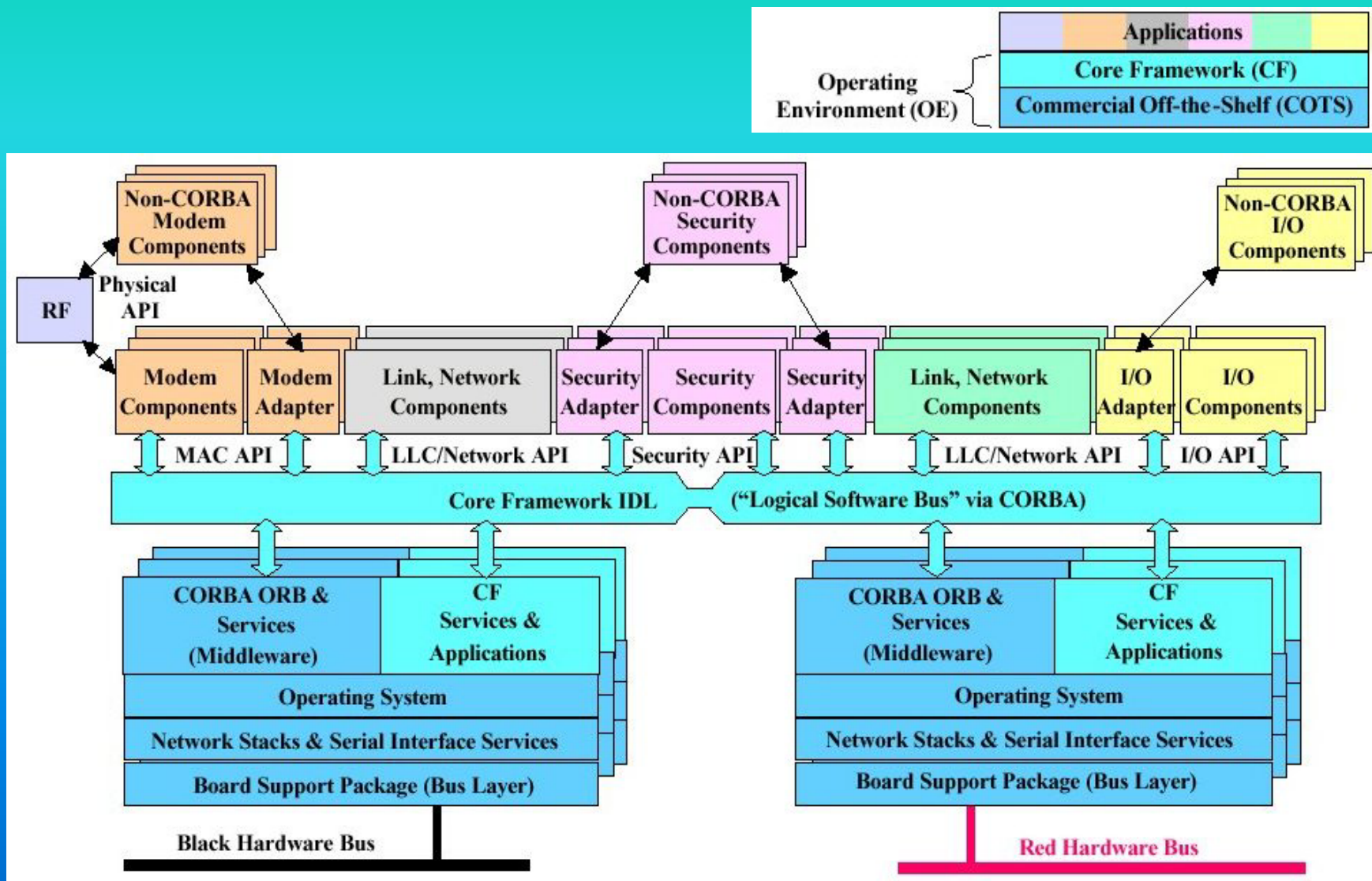 **Issues with Mixed L band and U/V Band**

- ## Baseband
  - *TRANSEC generation/Timing*
  - *RTT Response time*
  - *Bus loading/Timing*
  - *Enhanced Throughput Performance*
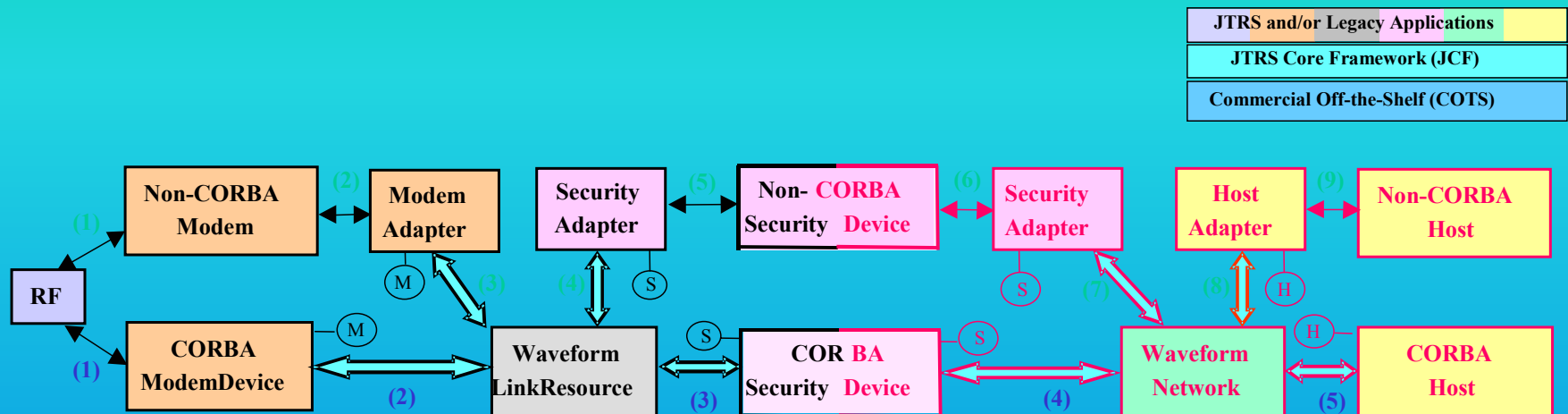
  "More power to the engines Scotty..."

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SCA v2.1 Software Structure

Example SCA Message Flows

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JTRS and/or Legacy Applications	
JTRS Core Framework (JCF)	
Commercial Off-the-Shelf (COTS)	

Message Reception Path (with Adapters)
(1) RF interface to Modem
(2) non-CORBA Modem Interface
(3) CORBA Interface to Waveform Link (M)
(4) CORBA Interface to Security Adapter (S)
(5) Black-side non-CORBA Security Interface
(6) Red-side non-CORBA Security Interface
(7) CORBA Interface to Waveform Network (S)
(8) CORBA Interface to Host Adapter (H)
(9) non-CORBA Host Interface

OTA Message Reception Path (without Adapters)
(1) RF Interface to Modem
(2) CORBA Interface to Waveform Link (M)
(3) CORBA Interface to Security (S)
(4) CORBA Interface to Waveform Network (S)
(5) CORBA Interface to Host (H)

Note: The design goal of a CORBA gateway "Adapter" is to define the CORBA side of the gateway such that the eventual replacement of the non-CORBA device and its Adapter does not change the JTRS Core Framework CORBA interface.

Keys to Compliance

- **MMDA has to have more than Software independence…….it must be functionally independent**

- **Graceful degradation of functionality as failures or performance shortfall occur**

- **Stress Testing of both Software and Hardware at each design and integration phase**
  - *Discover Maximum performance limits*
  - *Margin Adjustments for Cost reduction or performance enhancements*

- **Identify Keys for minimizing impact or re-qualification**
  - *Performance Improvements*
  - *New or added Functionality*

MMDA Design and Test Keys

Software

- **Modified OSIL/CORBA Design**

- **Early Software testing to eliminate SW-SW interface issues**

- **Early SW Testing on Target**

- **Early Stress Testing of SW**
  - *Throughput*
  - *Memory*
  - *HW/SW Interface*

Hardware
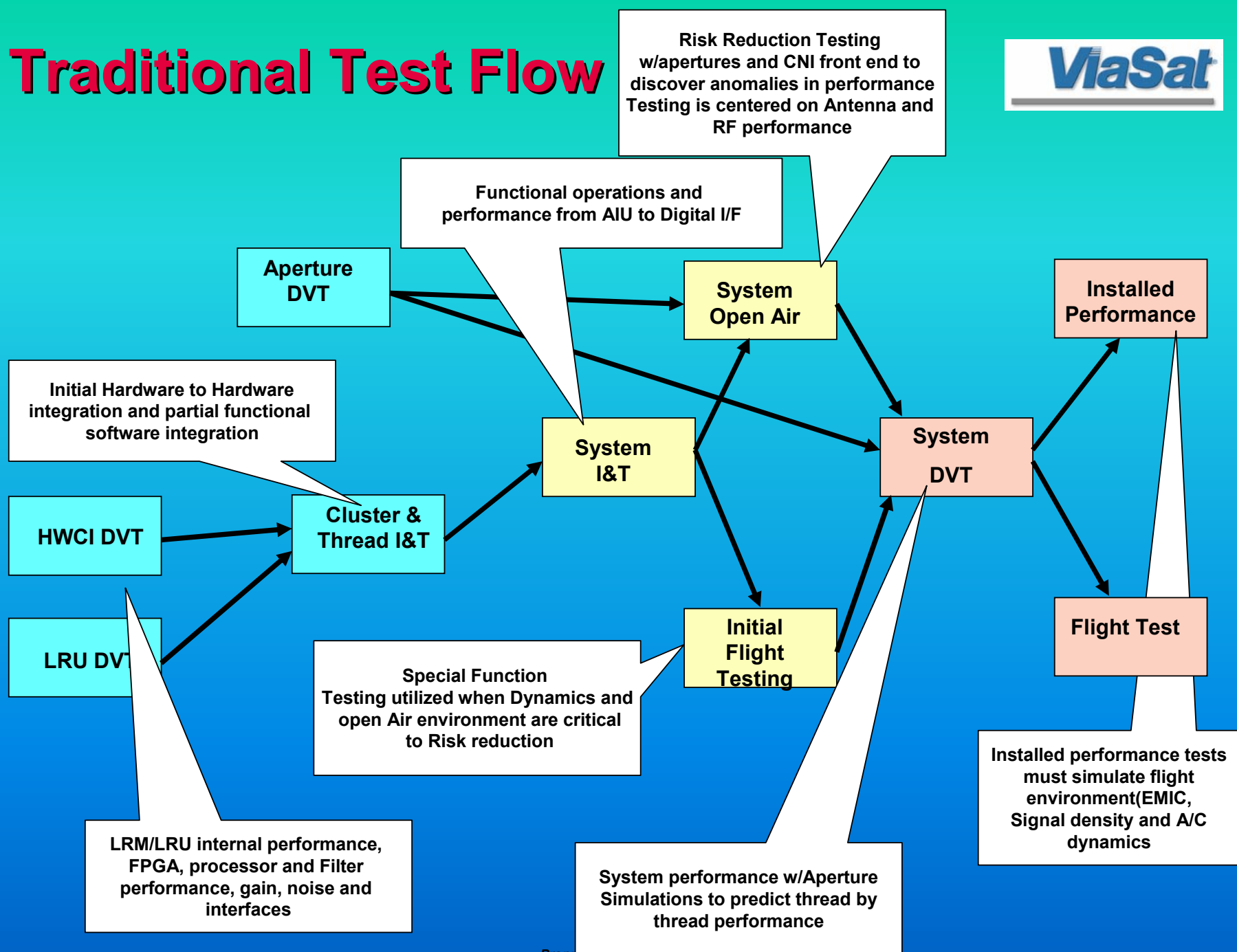
- **Standardized, open Bus Structure**

- **Low Level Stress testing of hardware and FPGA to break point**
  - *High Bus Traffic*
  - *Message Collision*
  - *Illegal Messages*
  - *Throughput with substandard HW performance*

- **Interface Testing with failed or corrupted HW installed**

**Functional Performance Testing with
Failed HW and Software or sub par performing Functions**

Traditional Test Flow

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Risk Reduction Testing w/apertures and CNI front end to discover anomalies in performance Testing is centered on Antenna and RF performance

Functional operations and performance from AIU to Digital I/F

Aperture DVT

System Open Air

Installed Performance

Initial Hardware to Hardware integration and partial functional software integration

System I&T

System DVT

HWCI DVT

Cluster & Thread I&T

LRU DVT

Special Function Testing utilized when Dynamics and open Air environment are critical to Risk reduction

Initial Flight Testing

Flight Test

LRM/LRU internal performance, FPGA, processor and Filter performance, gain, noise and interfaces

System performance w/Aperture Simulations to predict thread by thread performance

Installed performance tests must simulate flight environment(EMIC, Signal density and A/C dynamics

Qualification Plan Approach

- **Define Test Objectives**
  - *HW SRU Level*
  - *SW Module Level*
  - *Infrastructure Level*
  - *System Integration*
  - *Design Verification Testing*
  - *Qualification Testing*

- **Identify Key components of independent qualification**

- **Compare and analyze traditional Qualification programs with Software Defined Radio's**

- **Analyze final Architecture against qualification plan**
  - *Architecture and Qualification plan are intimately linked*

Enroll Certifying agencies in Test and Qualification process early!!!!!
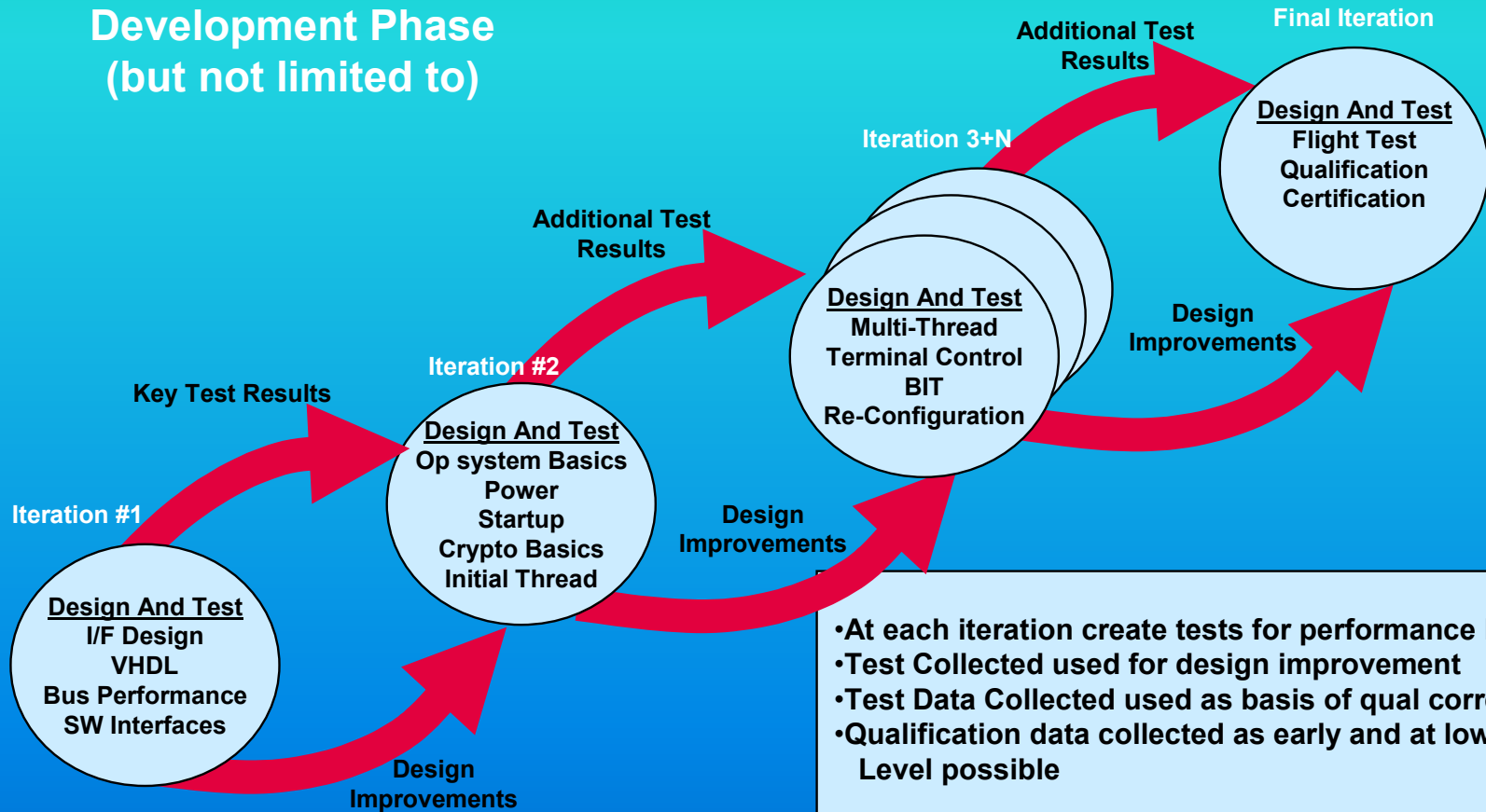
Qualification Risk Reduction

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- **Traditional Approach does not test beyond specification limits**

- **Test Early….Test Often**
  - *Independence of software from hardware*
  - *Functional independence*
  - *Key interfaces verified to open architecture standards*

- **Stress testing of Busses, power, and key performance areas**

- **Test to Failure**
  - *Discovery of performance limits of both software and hardware*
  - *Manufacturing and design margins*

- **Performance in the presence of Failures**
  - *Addition of new functions in environment with sub optimum performance*
  - *Proves independence of each of the key functional elements in the system*

Iterative Design, Test and Risk Reduction to Qualification

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Risks addressed at each Development Phase (but not limited to)

Realistic Test Environment

Final Iteration

Additional Test Results

Iteration 3+N

Design And Test
Flight Test
Qualification
Certification

Additional Test Results

Design Improvements

Design And Test
Multi-Thread
Terminal Control
BIT
Re-Configuration

Iteration #2

Key Test Results

Design And Test
Op system Basics
Power
Startup
Crypto Basics
Initial Thread

Design Improvements

Iteration #1

Design And Test
I/F Design
VHDL
Bus Performance
SW Interfaces

Design Improvements

- At each iteration create tests for performance limits
- Test Collected used for design improvement
- Test Data Collected used as basis of qual corrections
- Qualification data collected as early and at lowest Level possible

MMDA Product Maturity/System Buildup

MMDA System Certification

- **Certification of functions**
  - *Collection of Flight test, ground test and software qualification testing*
  - *Data analysis of test results*
  - *Supporting Analysis for requirements not directly testable*
  - *Data package and documentation preparation*
  - *Follow up on deficiencies and anomalies*
- **Data Collection taken from HWCI DVT through system integration to "end to end" testing**
  - *Certification documentation generated as early as feasible*
- **Certification dry runs conducted early to determine any performance shortfalls**
- **Certification of waveforms conducted individually and can be completed independently of other qualification tests**

Principal Qualification Concerns

- **Definition of testable requirements during the systems Engineering Phase of Development**

- **Qualification roadmap supporting Iterative Development and Testing**
  - *Provides path for future enhancements that minimize qualification risk and schedule (cost)*

- **Test Objectives defined early in the development cycle**
  - *Test Keyed to each phase of development and integration*

- **Define Key Technical Performance Measures Early in Program Development**